Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A method of phase splitting for generating multi-phase clocks having the same frequency and predetermined phase differences between one another, comprising:

a plurality of reference clocks each generating an output of a first frequency having a first phase difference from other reference clocks; and

for each of the plurality of reference clocks, utilizing a plurality of periods in the output of ~~each~~ a single reference clock to generate a plurality of output clocks each having a second frequency at a second phase difference from other output clocks generated by said single reference clock, each period of the second frequency being equal to the sum of the plurality of periods utilized in the output of ~~the~~ said single reference clock ~~clocks.~~;

wherein the first phase difference is a multiple of the second phase difference.

Claim 2 (Previously Presented): The method of claim 1 wherein the first frequency is a multiple of the second frequency.

Claim 3 (Currently Amended): The method of claim 1 ~~wherein the first phase difference is a multiple of the second phase difference,~~ wherein a ratio of the first phase difference to the second phase difference is the same as a ratio of the plurality of reference clocks to the plurality of output clocks.

Claim 4 (Previously Presented): The method of claim 1 wherein when the first frequency is N times the second frequency, the method further comprises triggering periods of

the second frequency according to the plurality of periods utilized in the output of one of the reference clocks at intervals of at least (N-1) period.

Claim 5 (Currently Amended): The method of claim 1 wherein if the output of two reference clocks have the first phase difference of 360 degrees, the two reference clocks are essentially the same, and when using the two reference clocks to generate two corresponding output clocks, the two corresponding output clocks are triggered by different periods of one reference clock.

Claim 6 (Previously Presented): The method of claim 1 wherein two of the plurality of reference clocks are a first reference clock and a second reference clock, the method further comprising:

determining a first reference period of the first reference clock and also finding a first reference period in the second reference clock lagging the first reference period of the first reference clock;

dividing the frequency of the first reference clock at a time point corresponding to the first reference period of the first reference clock in order to generate an output clock; and

dividing the frequency of the second reference clock at a time point corresponding to the first reference period of the second reference clock in order to generate another output clock.

Claim 7 (Previously Presented): The method of claim 6 wherein the first reference clock leads the second reference clock by the first phase difference.

Claim 8 (Previously Presented): The method of claim 1 wherein the periods of each output clock are triggered by reference periods of a corresponding reference clock apart from other reference clocks by at least one or a plurality of periods of the

corresponding reference clock wherein if a first period of one of the output clocks is triggered by a first reference period of a corresponding reference clock, a second period of said one of the output clocks would be triggered by a reference period lagging the first reference period by the first phase difference in ~~the~~ a second reference clock, the second period of said one of the output clocks lagging the first period of said one of the output clocks by the second phase difference.

Claim 9 (Previously Presented): The method of claim 1 wherein ~~the~~ two reference clocks are a first reference clock and a second reference clock, the method further comprising:

selecting a first reference period in the first reference clock;

in the second reference clock, stopping a reference period lagging the first reference period to generate a corresponding intermediate clock so that each reference period of the corresponding intermediate clock will lag the first reference period in the first reference clock; and

dividing the frequency of the first reference clock and the corresponding intermediate clock to generate two corresponding output clocks.

Claim 10 (Currently Amended): A multi-phase clock-generating circuit for generating two output clocks of the same frequency with a predetermined phase difference between each other, comprising:

a clock generator for generating two reference clocks having a same frequency that is a multiple greater than 1 of the frequency of the two output clocks, the two reference clocks having a predetermined reference phase difference between each other; and

a phase interpolator for generating ~~the~~ two corresponding output clocks wherein each period of these two output clocks is triggered by a corresponding reference period of one of the two reference clocks, which is apart from other

reference periods of said one of the two reference clocks by at least one or a plurality of periods of said one of the two reference clocks.

Claim 11 (Previously Presented): The multi-phase clock-generating circuit of claim 10 wherein the two reference clocks are a first reference clock and a second reference clock, the multi-phase clock-generating circuit further comprising:

a sequence triggering module for stopping a reference period of the second reference clock lagging a first reference period of the first reference clock to generate a corresponding intermediate clock; and

a frequency division module for dividing the frequency of the first reference clock and the corresponding intermediate clock to generate two corresponding output clocks; wherein each reference period of the corresponding intermediate clock lags the first reference period of the first reference clock.

Claim 12 (Previously Presented): The multi-phase clock-generating circuit of claim 11 wherein the first reference clock leads the second reference clock by the predetermined reference phase difference.

Claim 13 (Previously Presented): The multi-phase clock-generating circuit of claim 10 wherein two reference clocks are a first reference clock and a second reference clock, and the phase interpolator comprises:

a sequence triggering module for finding in the second reference clock a first reference period lagging a first reference period of the first reference clock, and producing a corresponding reset signal at a time corresponding to the first reference period of the second reference clock;

a first frequency divider for generating an output clock by dividing the frequency of the first reference clock; and

a second frequency divider for generating the other output clock by dividing the

frequency of the second reference clock after receiving the corresponding reset signal.

Claim 14 (Previously Presented): The multi-phase clock-generating circuit of claim 13 wherein the first frequency divider and the second frequency divider are triggered by rising edges of the first and second reference clocks respectively.

Claim 15 (Original): The multi-phase clock-generating circuit of claim 10 wherein the frequency of the reference clocks is a multiple of the frequency of the output clocks.

Claim 16 (Previously Presented): The multi-phase clock-generating circuit of claim 10 wherein the predetermined reference phase difference is plural times an output phase difference between outputs of the output clocks, and a ratio of the predetermined reference phase difference to the output phase difference is the same as a ratio of the frequency of the two reference clocks to the frequency of the output clocks.

Claim 17 (Currently Amended): A method of phase-splitting for generating two output clocks of the same frequency with a predetermined phase difference between each other, comprising:

generating a first reference clock having a frequency that is a multiple greater than 1 of a frequency of a corresponding output clock, ~~and~~ <u>a period of the corresponding output clock being</u> substantially equal to an integer multiple of a reference period of the first reference clock; and

triggering periods of different said two output clocks by the reference period of the corresponding reference clock to generate the two output clocks.

Claim 18 (Currently Amended): The method of claim 17 wherein the predetermined

phase difference of the two output clocks is ~~not essentially equal to~~ between 0 and 360 degrees.

Claim 19 (Currently Amended): The method of claim 17 wherein the predetermined phase difference of the two output clocks is ~~not essentially equal to~~ between 0 and 180 degrees or between 180 and 360 degrees.

Claim 20 (Previously Presented): The method of claim 17 wherein if the frequency of the reference clock is N times that of the corresponding output clock, the predetermined phase difference of the two output clocks is a multiple of 360/N degrees.

Claim 21 (Previously Presented): The method of claim 17 wherein frequency division is triggered by the reference period of the first reference clock to generate an output clock, a second reference period lagging the reference period of the first reference clock starting frequency division to generate another output clock.

Claim 22 (Previously Presented): The method of claim 17 wherein a third output clock can be produced, the third output clock having the same frequency as the two output clocks but different phase, the method further comprising:

generating a second reference clock having the same clock frequency but a different phase as the first reference clock; and

triggering each period of the third output clock according to each period of the second reference clock;

wherein output of the third output clock is of the same frequency as said two output clocks and has the predetermined phase difference from said two output clocks.